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Comparative Analysis of A Reduced Multilevel Inverter Using Different Modulation Technique

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***Abstract*—The multilevel inverters performing power conversion in multiple voltage steps to achieve better power quality, lower switching losses, higher electromagnetic compatibility, and superior voltage capability. Multilevel Inverter (MLI) provides high power capability, with low output harmonics and low commutation losses. In industries they are widely applicable in large number of applications. This paper proposed a new multilevel inverter structure with low output harmonics. In this paper the number of switching device is less as compare to the conventional multilevel inverter. It consists of an H-bridge inverter which produces multilevel output voltage by switching DC voltage sources in series and parallel. This topology produces a significant reduction in the number of power devices. This advance topology generates large number of voltage levels with the minimum number of switches. The proposed topology also reduces the total harmonic distortion (THD) of its output waveform. This paper also represent circuit configuration, theoretical operation and MATLAB based simulation results.**

Keywords— Multilevel inverter, Switched series parallel, H-bridge, PWM

I. INTRODUCTION

Power electronic converters, mainly DC/AC PWM inverters have been dispersion their range of use in industry because they provide reduced energy consumption, better system efficiency, enhanced quality of product, better maintenance, and so on.

For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1, 2, 3]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as pumps, conveyors, laminators, compressors, mills, fans, blowers, and so on. As a cost effective resolution, multilevel converter not only achieve high power ratings, but also permit the use of low power application in renewable energy sources such as wind, fuel cells, and photovoltaic which can be simply interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More recent applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12]. The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems [13], namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased.

Some kinds of series and/or parallel connections are necessary to defeat the problems of the limited voltage and current ratings of power semiconductors devices. In recent year, the multilevel inverters have received much more interest from the researcher in literature knowledge due to their ability to synthesize waveforms with an enhanced harmonic spectrum and to achieve higher voltages [14].

MLI are extensively used in many industrial applications such as static Var compensators, drive System and ac power supplies etc. Multilevel inverters have very important development for high power medium voltage AC drives. Fairly a lot of topologies have establish industrial approval; Diode clamped (DCMLI), Flying capacitors (FCMLI) and Cascade H-bridge (CHB) cells with separated DC source, numerous control and modulation strategies have been developed Pulse Width Modulation (PWM), Space Vector PWM, Selective harmonic eliminations and Sinusoidal PWM etc. One of the significant advantages of multilevel configuration is the harmonics reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [15, 16]. Multilevel inverters are used to drive many electrical machines such as Hybrid Electric Vehicles (HEVs) and Electric Vehicles (EVs) [17].

On the other hand, when inverter switches maintain high voltage, their switching frequency is limited. In this state, the output waveform of inverter is distorted and one of the main disadvantages is the great number of power semi-conductor switches needed. In a multilevel inverter low voltage rate switches can be utilized and each switch requires a related gate driver circuits. Due to this reason the overall system to be more costly and complex. So, in practical execution, minimizing the number of switches and gate driver circuits is very important.

This paper suggest a new topology for comparative analysis of a reduced multilevel inverter using different modulation technique with a high number of steps allied with a low number of switches and gate driver circuits for switches. In addition, for producing all levels (odd and even) at the output voltage, three techniques for obtained dc voltage and THD calculation are proposed. Finally, the paper includes simulation result to prove the probability of the proposed multilevel inverter [18].

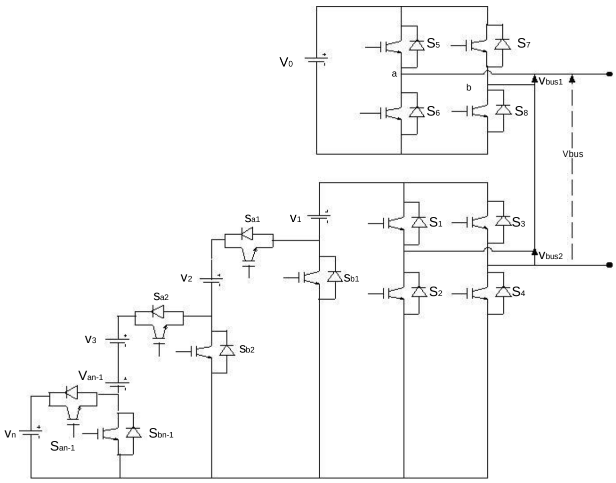
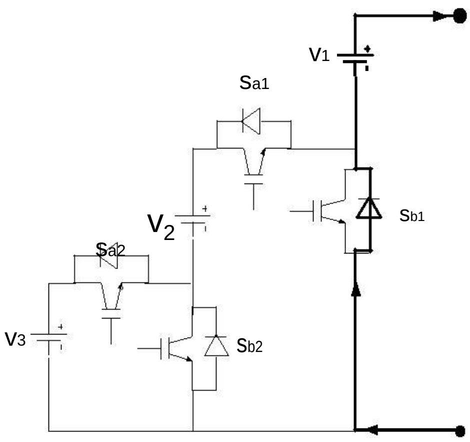
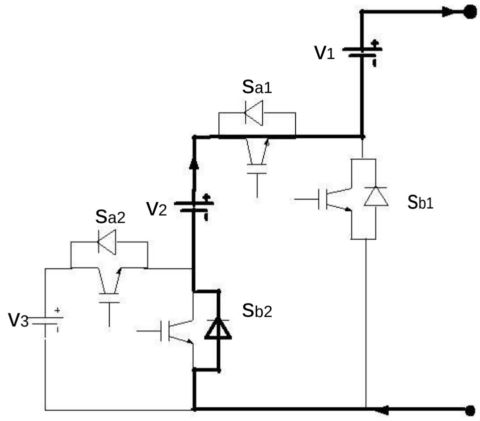


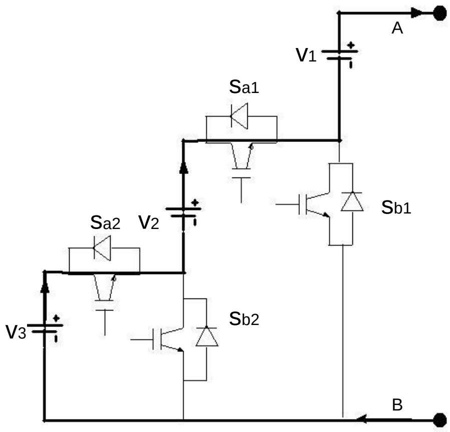
Fig.1.Structure of the proposed (4n+3)-levels inverter



(a)



(b)



(c)

Fig.2. Current flow of the proposed 19-level inverter by series conversion, (a) V_1 connected via the switch $S_{b1,}$ (b) V_1 and V_2 are connected in series, (c) V_1, V_2 and V_3 are connected in series [23].

II. THE PROPOSED TOPOLOGY

Power circuit topology of the proposed multilevel inverter is shown in Fig.1. As shown in this figure, inverter is constructed from two parts. Part one is an H-bridge inverter with DC voltage source equal to V_0 and part two is an inverter with DC voltage sources equal to V_k (k = 1, 2,…, n) . DC voltage sources V_0 ~V_n are independent each other, and it is assumed that V_0: V_{k} = 1: 2 (k = 1, 2,…, n). Switches S_{a1} ~ S_{an-1} and S_{b1} ~ S_{bn-1} are the switches which switch the DC voltage sources in series. The proposed inverter is driven by the hybrid modulation method [19]. Fig. 2 shows the series conversion of the DC voltage sources of the proposed 19-level (n = 4) inverter. When the switch Sb1 becomes ON, the current flows in the switch S_{b1},so the input of lower H-bridge is connect the voltage sourceV_1 (Fig. 2(a)).

As a result, the voltage VAB between the point A and the point B becomes VAB = V1 (Fig. 2(a)). On the other hand, when the switches Sa1 and Sb2 become ON and the other switches become OFF, the current flows in switches Sa1and Sb2 , which connect the voltage sources V1 and V2 in series and VAB = V1 +V2 (Fig. 2(b)). Finally, when the switches Sa1 and Sa2 become ON and other switches become OFF, the current flow in switches Sa1 and Sa2 , which connect the voltage sources V1~V3 in series and VAB = V1(Fig. 2(c)).

Using this series conversion of DC voltage sources, the lower H-bridge outputs Vbus2 in (2n +1)-level, while the upper H-bridge outputs V0 =Vbus1. The proposed multilevel inverter outputs (4n + 3) level by Vbus1 + Vbus2 or Vbus2 − Vbus1. In other conventional inverters such as CHB, DCMLI and FCMLI, a similar scheme can be used [20]. The proposed multilevel inverter requires the less number of switching devices than CHB, DCMLI and FCMLI. When the proposed inverter is applied to some application without reverse power flow, switches Sb1~Sbn−1 can be replaced by diodes.

For example, when a resistive load is connected to the output of the proposed inverter, the output current is accorded with the voltage phase. When the ratio of the voltages of the sources V_0 :V_k= 1:3 is assumed, the proposed inverter requires 12 devices for 19- level. When an inductive load is connected, the output current lags behind the output voltage. The proposed multilevel inverter requires the less number of switching devices than the DCMLI, FCMLI and CHB [21]. Therefore, a state is achieved when the direction of the current becomes reverse to the power sources.

III. MODULATION TECHNIQUES

In this section, the modulation method of the proposed inverter is explained for the 19-level inverter. Fig. 3 shows the modulation method of the proposed 19-level inverter. Multilevel converters are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: Level Shifted (LS-PWM), which includes Phase Opposition Disposition (POD-PWM), Phase Disposition (PD-PWM), and Alternative Phase Opposition Disposition (APOD-PWM) or they can be Phase Shifted (PS-PWM) [22].

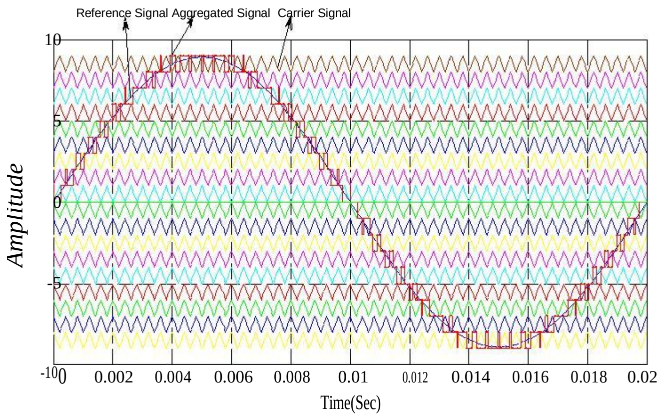


Fig.3. Associated waveforms for control and modulation of the proposed inverter through POD for n=4.

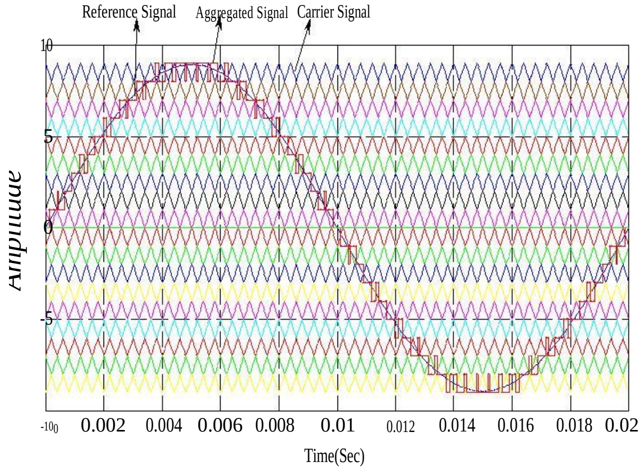


Fig.4. Associated waveforms for control and modulation of the proposed inverter through APOD for n=4.

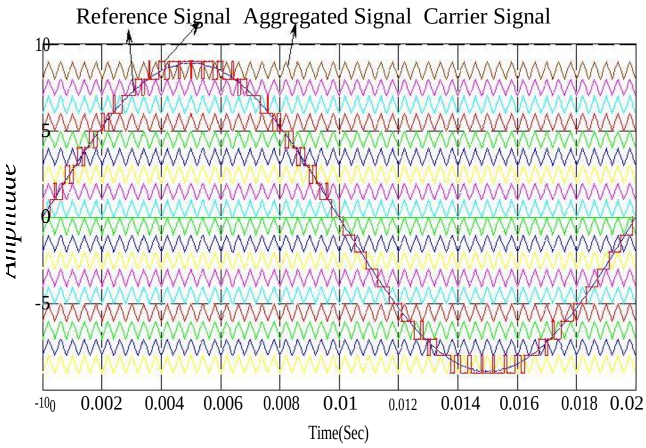


Fig.5. Associated waveforms for control and modulation of the proposed inverter through PD for n=4.

IV. SIMULATION RESULT

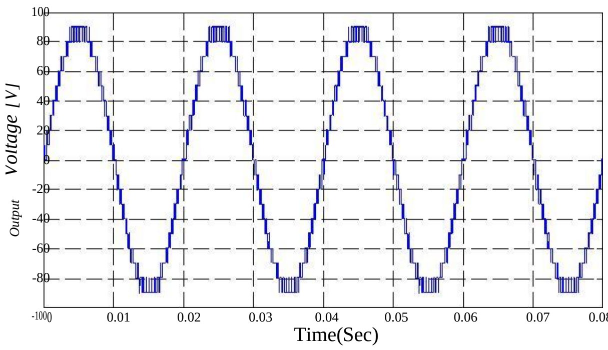


Fig.6. output voltage waveform Vout for 19-level

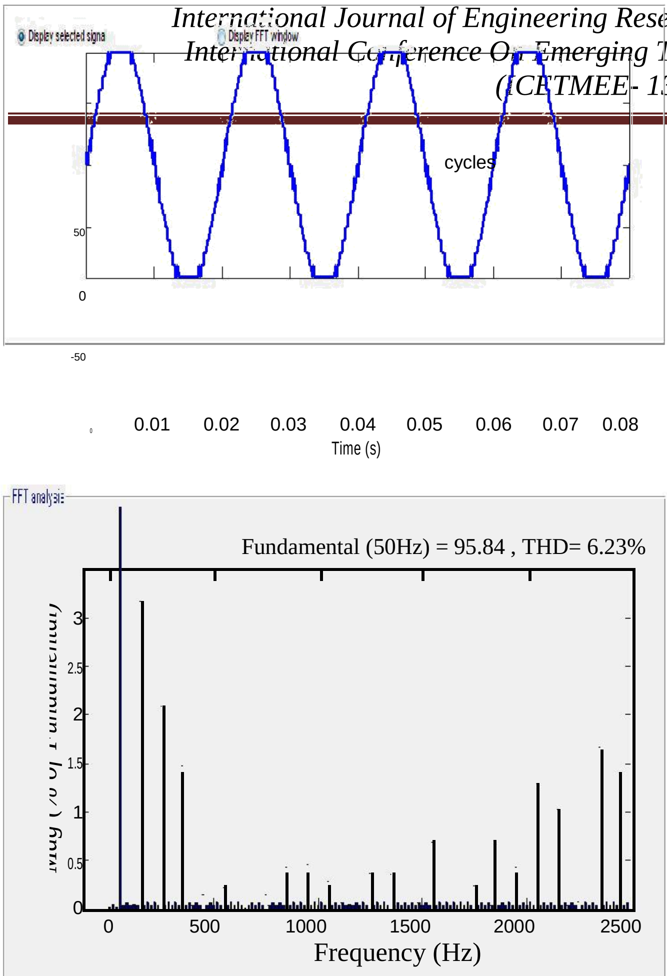


Fig.7. FFT analysis for output voltage waveforms Vout 19-level through POD

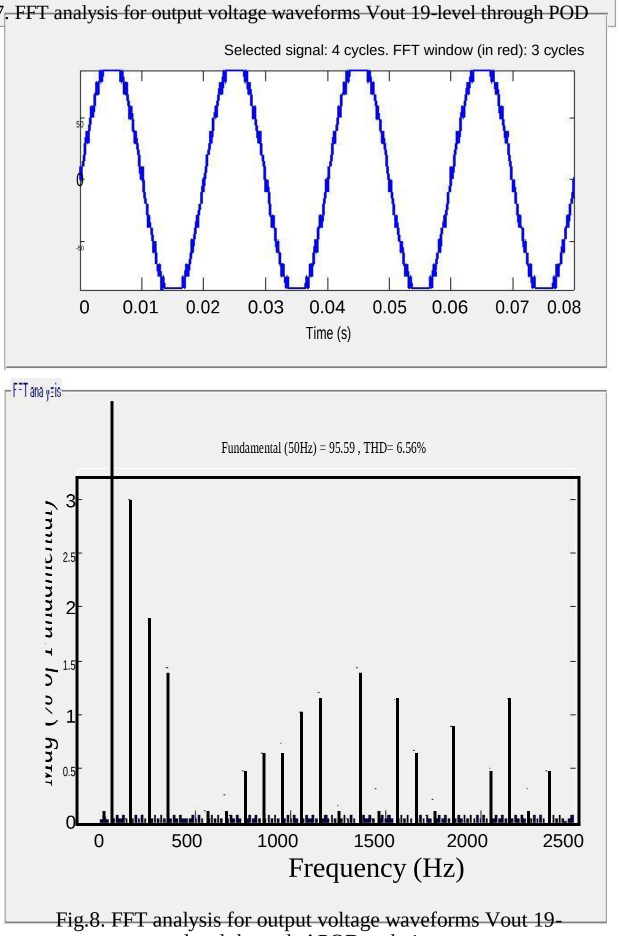


Fig.8. FFT analysis for output voltage waveforms Vout 19-level through APOD techniques

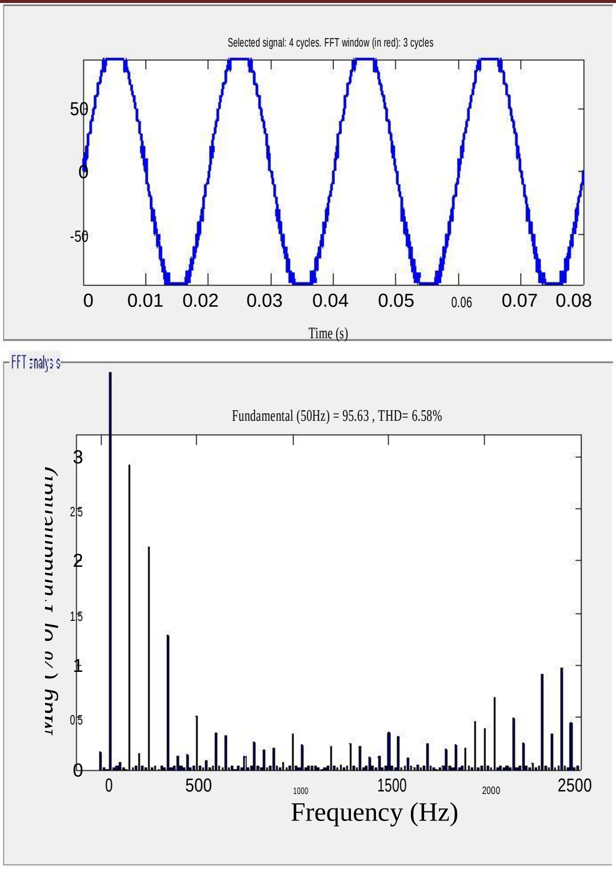


Fig.9. FFT analysis for output voltage waveforms Vout 19-level through PD techniques

TABLE I. COMPARISON OF THE CALCULATED THD

Modulation Index	POD PWM % THD	PD PWM % THD	APOD PWM % THD
1.1	6.23	6.58	6.56
1.0	7.21	6.75	6.71
0.90	7.67	6.97	6.91

V. CONCLUSION

A Comparative Analysis of a reduced multilevel inverter Using Different Modulation Technique has been proposed in this paper. The most important feature of this system is suitable for increasing and getting higher number of output level with less number of switches. The result of this method is to decrease the number of switches, losses, cost and also size. The multilevel inverter generates nearly sinusoidal output voltage with very low harmonic content with the help of this proposed topology. So the output waveform of inverter is enhanced than the conventional multilevel inverter from THD approach.

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